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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PWU, JEFFREY C

ART UNIT	PAPER NUMBER
2143	

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DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,702	BUCH ET AL.	
	Examiner	Art Unit	
	Jeffrey Pwu	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-38 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/30/2001.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being over Ramaswamy et al. (U.S. 6,510,164).

Ramaswamy et al. disclose claims:

1. A method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing N NICs (Network Interface Cards) (37_1, 37_2), a first one of the N NICs being dedicated to receiving an incoming data stream (13);

binding an interrupt from the first one of the N NICs to a first one of the N processors (see kernel-Deferred Procedure calls are managed in NT by a DPC kernel objects; also see col.11, line 30-col.113, line 38);

binding an interrupt for an nth NIC to an nth processor, wherein 0<n<=N (col.3, lines 10-67); and

binding a DPC (Deferred Procedure Call) for the nth NIC to the nth processor (DPC to processor interrupt is an inherent feature of NT).

2. The method of claim 1, further comprising tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer (24, 17).

3. The method of claim 1, further comprising binding P server threads to specific ones of second through N processors, wherein P is a positive integer (col.13, line 61-col.14, line 20).

4. The method of claim 2, further comprising binding P server threads to specific ones of second through N processors, wherein P is a positive integer (col.13, line 61-col.14, line 20).

5. The method of claim 1, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2

caches (col.11, line 30-46).

6. The method of claim 2, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

7. The method of claim 3, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

8. The method of claim 4, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

9. A method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising: implementing N NICs (Network Interface Cards); and tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer and wherein 0<n<=N (figs.2, 3, & 7).

10. The method of claim 9, further comprising binding P server threads to specific ones of second through N processors, wherein P is a positive integer (col.13, line 61-col.14, line 20).

11. The method of claim 10, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

12. The method of claim 9, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

13. A method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising: implementing N NICs (Network Interface Cards); and binding P server threads to specific ones of a second through N processors (see kernel-Deferred Procedure calls are managed in NT by a DPC kernel objects; also see col.11, line 30-col.113, line 38);

14. The method of claim 13, further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2

caches (col.11, line 30-46; fig.2).

15. A method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising: implementing L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (col.11, line 30-46; fig.2).

16. The method of claim 5, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.5, line 41-col.6, line 3).

17. The method of claim 6, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.5, line 41-col.6, line 3).

18. The method of claim 7, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.5, line 41-col.6, line 3; col.7, lines 15-40).

19. The method of claim 8, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.7, lines 15-40).

20. The method of claim 11, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.7, lines 15-40).

21. The method of claim 14, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.7, lines 15-40).

22. The method of claim 15, further comprising improving L1 cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers (col.7, lines 15-40).

23. A multiprocessor data server comprising: N processors, wherein N is an integer greater than or equal to 2; N NICs (Network Interface Cards), a first one of said N NICs being dedicated to receiving an incoming data stream; wherein an interrupt from the first one of said N NICs is bound to a first one of said N processors; and wherein an interrupt for an nth NIC is bound to an nth processor, 0<n<=N; and wherein a DPC (Deferred Procedure Call) for said nth NIC is bound to said nth processor (claim 23 is similarly rejected as in claims 1-22).

24. The multiprocessor data server of claim 23, further comprising M client connections, wherein said M client connections are tightly coupled to said nth processor via said nth NIC, M being a positive integer (claim 24 is similarly rejected as in claims 1-22).

25. The multiprocessor data server of claim 23, further comprising P server threads, wherein said

P server threads are bound to specific ones of a second through N processors (claim 25 is similarly rejected as in claims 1-22).

26. The multiprocessor data server of claim 24, further comprising P server threads, wherein said P server threads are bound to specific ones of a second through N processors (claim 26 is similarly rejected as in claims 1-22).

27. The multiprocessor data server of claim 23, further comprising L1 (Level 1) and L2 (Level 2) caches for each of said N processors, wherein instructions and temporal data are stored in said L2 caches of said N processors, and wherein non-temporal data is stored in L1 caches of said N processors, bypassing the L2 caches (claim 27 is similarly rejected as in claims 1-22).

28. The multiprocessor data server of claim 24, further comprising L1 (Level 1) and L2 (Level 2) caches for each of said N processors, wherein instructions and temporal data are stored in said L2 caches of said N processors, and wherein non-temporal data is stored in L1 caches caches of said N processors, bypassing the L2 caches (claim 28 is similarly rejected as in claims 1-22).

29. The multiprocessor data server of claim 25, further comprising L1 (Level 1) and L2 (Level 2) caches for each of said N processors, wherein instructions and temporal data are stored in said L2 caches of said N processors, and wherein non-temporal data is stored in L1 caches caches of said N processors, bypassing the L2 caches (claim 29 is similarly rejected as in claims 1-22).

30. The multiprocessor data server of claim 26, further comprising L1 (Level 1) and L2 (Level 2) caches for each of said N processors, wherein instructions and temporal data are stored in said L2 caches of said N processors, and wherein non-temporal data is stored in L1 caches caches of said N processors, bypassing the L2 caches (claim 30 is similarly rejected as in claims 1-22).

31. A program storage device, readable by a machine, embodying a program of instructions executable by the machine to perform a method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising: implementing N NICs (Network Interface Cards), a first one of the N NICs being dedicated to receiving an incoming data stream; binding an interrupt from the first one of the N NICs to a first one of the N processors; binding an interrupt for an nth NIC to an nth processor, wherein 0<n<=N; and binding a DPC (Deferred Procedure Call) for the nth NIC to the nth processor (claim 31 is similarly rejected as in claims 1-22).

32. The program storage device of claim 31, the method further comprising tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer (claim 32 is similarly rejected as in claims 1-22).

33. The program storage device of claim 31, the method further comprising binding P server threads to specific ones of second through N processors, wherein P is a positive integer (claim 33 is similarly rejected as in claims 1-22).

34. The program storage device of claim 32, the method further comprising binding P server threads to specific ones of second through N processors, wherein P is a positive integer (claim 33 is similarly rejected as in claims 1-22).

35. The program storage device of claim 31, the method further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (claim 35 is similarly rejected as in claims 1-22).

36. The program storage device of claim 32, the method further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (claim 36 is similarly rejected as in claims 1-22).

37. The program storage device of claim 33, the method further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (claim 37 is similarly rejected as in claims 1-22).

38. The program storage device of claim 34, the method further comprising: defining L1 (Level 1) and L2 (Level 2) caches for each of the N processors; storing instructions and temporal data in

L2 caches of the N processors; and storing non-temporal data in L1 caches of the N processors, bypassing the L2 caches (claim 38 is similarly rejected as in claims 1-22).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey Pwu whose telephone number is 571 272-6798. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 571 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 3, 2005

JEFFREY PWU
PRIMARY EXAMINER